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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,126	11/27/2001	Robert Conrad Malkemes	SAR 13895A	1964
28166	7590	04/01/2005		
MOSER, PATTERSON & SHERIDAN, LLP /SARNOFF CORPORATION 595 SHREWSBURY AVENUE SUITE 100 SHREWSBURY, NJ 07702			EXAMINER LUGO, DAVID B	
			ART UNIT	PAPER NUMBER
			2637	

DATE MAILED: 04/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

09/995,126

**Applicant(s)**

MALKEMES ET AL.

**Examiner**

David B. Lugo

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 November 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 November 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>3/14/02</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Objections***

1. Claim 13 is objected to because of the following informalities:

Claim 13 recites the limitation "the tuners" in line 1. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

### ***Double Patenting***

2. Claims 1 and 3 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 7 of copending Application No. 09/776,078 in view of Win et al. U.S. Patent 6,804,312.

Regarding claim 1 of the instant application, claim 7 of the '078 application disclose receiving a plurality of spatially diverse replicas of an RF signal, and adaptively combining the spatially diverse replicas to generate an equalized signal.

Claim 7 of the '078 application does not expressly disclose that the receiver may be implemented in a computer readable storage medium containing a program.

However, it is well known in the art to implement a digital receiver using a program contained in computer readable storage medium. For instance, Win et al. disclose that a digital receiver for spatial processing that may be implemented with various software techniques (col. 11, lines 45-55).

It would have been obvious to one of ordinary skill in the art to implement the receiver using a software implementation where a computer program is stored in computer readable storage medium as a matter of design choice, as software and hardware implementations are well-recognized art equivalents.

Further regarding claim 1 of the instant application, claim 7 of the '078 application include limitations specifying what the combining step includes. It would have been obvious to one of ordinary skill in the art to remove those limitations along with their specified functions.

Regarding claim 3 of the instant application, claim 7 of the '078 application further includes spatially equalizing the spatially diverse replicas, combining the replicas, generating a symbol signal using the combined signal, temporally equalizing the combined signal using a DFE, and adapting the spatial equalizing and temporal equalizing steps to the symbol signal.

This is a provisional obviousness-type double patenting rejection.

3. Claims 4, 5, 7-9 and 11-13 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 3 of copending Application No. 09/776,078 in view of Win et al.

Regarding claims 4 and 9 of the instant application, claim 7 of the '078 application disclose receiving a plurality of spatially diverse replicas of an RF signal, and adaptively combining the spatially diverse replicas to generate an equalized signal.

Claim 7 of the '078 application does not expressly disclose that the combiner is part of an integrated circuit or a digital signal processor.

However, it is well known in the to implement portions of a digital receiver using integrated circuits and digital signal processors. For instance, Win et al. disclose that digital receivers may be implemented with various circuit and software techniques, including integrated circuits and DSPs (col. 11, lines 45-55).

It would have been obvious to one of ordinary skill in the art to implement the combiner of Tsujimoto using an integrated circuit or a DSP as a matter of design choice as software and hardware implementations are well-recognized art equivalents.

Further regarding claims 4 and 9 of the instant application, claim 7 of the '078 application include limitations specifying what the combiner includes. It would have been obvious to one of ordinary skill in the art to remove those limitations along with their specified functions.

Regarding claim 5 of the instant application, Win et al. disclose that the integrated circuit may be an ASIC.

Regarding claims 7 and 11 of the instant application, claim 7 of the '078 application further includes spatially equalizing the spatially diverse replicas, combining the replicas, generating a symbol signal using the combined signal, temporally equalizing the combined signal using a DFE, and adapting the spatial equalizing and temporal equalizing steps to the symbol signal.

Regarding claim 8 of the instant application, Win further discloses the combination of ASICs and microcontrollers for performing various spatial processing operations (col. 11, lines 45-55). Use of a programmable ASIC configured by a microcontroller for implementing the combining means is deemed a design consideration that fails to patentably distinguish.

Regarding claim 12 of the instant application, Win further discloses the combination of DSPs and microcontrollers for performing various spatial processing operations (col. 11, lines 45-55). Use of a general purpose DSP configured by a microcontroller for implementing the combining means is deemed a design consideration that fails to patentably distinguish.

Regarding claim 13 of the instant application, implementing tuners of the receiver and the DSP as an ASIC is deemed a design consideration that fails to patentably distinguish.

This is a provisional obviousness-type double patenting rejection.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 2, 4-6, 8-10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsujimoto U.S. Patent 5,524,125 in view of Win et al. U.S. Patent 6,804,312.

6. Regarding claim 1, Tsujimoto discloses a receiver in Figure 2 for receiving a radio frequency signal comprising receiving a plurality of spatially diverse replicas of the RF signal (diversity reception signals 1 and 2), and adaptively combining the spatially diverse replicas to generate an equalized signal, Sd.

Tsujimoto does not expressly disclose that the receiver may be implemented in a computer readable storage medium containing a program.

However, it is well known in the art to implement a digital receiver using a program contained in computer readable storage medium. For instance, Win et al. disclose that a digital receiver for spatial processing that may be implemented with various software techniques (col. 11, lines 45-55).

It would have been obvious to one of ordinary skill in the art to implement the receiver of Tsujimoto using a software implementation where a computer program is stored in computer

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readable storage medium as a matter of design choice, as software and hardware implementations are well-recognized art equivalents.

7. Regarding claim 2, Tsujimoto further teaches spatially equalizing each of the spatially diverse replicas in equalizers 101, 102, combining the spatially equalized replicas to form a combined signal via combiner 158, generating a symbol error signal from the combined signal using symbol slicer circuit 109, temporally equalizing the combined signal via decision feedback equalizer 105, and adapting the spatial and temporal equalizing steps to the symbol error signal via tap control circuits 103, 104, 106 (see col. 7, lines 1-46).

8. Regarding claim 4, Tsujimoto discloses an apparatus for receiving a radio frequency signal comprising a front end for receiving diverse replicas of the RF signal, selecting the RF signal from a frequency band, and digitizing the selected RF signal, as described in col. 6, lines 61-65, and a combiner 158 for combining the spatially diverse replicas of the RF signal to generate an equalized RF signal.

Tsujimoto does not expressly disclose that the combiner is part of an integrated circuit.

However, it is well known in the to implement portions of a digital receiver using integrated circuits. For instance, Win et al. disclose that digital receivers may be implemented with various circuit and software techniques, including integrated circuits (col. 11, lines 45-55).

It would have been obvious to one of ordinary skill in the art to implement the combiner of Tsujimoto using an integrated circuit as a matter of design choice as software and hardware implementations are well-recognized art equivalents.

9. Regarding claim 5, Win et al. disclose that the integrated circuit may be an ASIC.

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10. Regarding claim 6, Tsujimoto further teaches spatially equalizing each of the spatially diverse replicas in feed forward equalizers 101, 102, combining the spatially equalized replicas to form a combined signal via combiner 158, generating a symbol error signal from the combined signal using symbol slicer circuit 109, temporally equalizing the combined signal via decision feedback equalizer 105, and adapting the spatial and temporal equalizing steps to the symbol error signal via tap control circuit 103, 104, 106 (see col. 7, lines 1-46).

11. Regarding claim 8, Win further discloses the combination of ASICs and microcontrollers for performing various spatial processing operations (col. 11, lines 45-55). Use of a programmable ASIC configured by a microcontroller for implementing the combining means is deemed a design consideration that fails to patentably distinguish over the prior art of record.

12. Regarding claim 9, Tsujimoto discloses an apparatus for receiving a radio frequency signal comprising a front end for receiving diverse replicas of the RF signal, selecting the RF signal from a frequency band, and digitizing the selected RF signal, as described in col. 6, lines 61-65, and a combiner 158 for combining the spatially diverse replicas of the RF signal to generate an equalized RF signal.

Tsujimoto does not expressly disclose that the combiner is part of a digital signal processor.

However, it is well known in the to implement portions of a digital receiver using DSPs. For instance, Win et al. disclose that digital receivers may be implemented with various circuit and software techniques, including DSPs (col. 11, lines 45-55).

It would have been obvious to one of ordinary skill in the art to implement the combiner of Tsujimoto using a DSP as a matter of design choice as software and hardware implementations are well-recognized art equivalents.

13. Regarding claim 10, Tsujimoto further teaches spatially equalizing each of the spatially diverse replicas in feed forward equalizers 101, 102, combining the spatially equalized replicas to form a combined signal via combiner 158, generating a symbol error signal from the combined signal using symbol slicer circuit 109, temporally equalizing the combined signal via decision feedback equalizer 105, and adapting the spatial and temporal equalizing steps to the symbol error signal via tap control circuit 103, 104, 106 (see col. 7, lines 1-46).

14. Regarding claim 12, Win further discloses the combination of DSPs and microcontrollers for performing various spatial processing operations (col. 11, lines 45-55). Use of a general purpose DSP configured by a microcontroller for implementing the combining means is deemed a design consideration that fails to patentably distinguish over the prior art of record.

15. Regarding claim 13, implementing tuners of the receiver and the DSP as an ASIC is deemed a design consideration that fails to patentably distinguish over the prior art of record.

16. Claims 3, 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsujimoto in view of Win et al., and further in view of Liang et al. U.S. Patent 6,314,147.

17. Regarding claim 3, Tsujimoto discloses a receiver as disclosed above, and further teaches spatially equalizing each of the spatially diverse replicas in equalizers 101, 102, combining the spatially equalized replicas to form a combined signal via combiner 158, generating a symbol error signal from the combined signal via circuit 109, temporally equalizing the combined signal

via decision feedback equalizer 105, and adapting the spatial and temporal equalizing steps to the symbol error signal via tap control circuits 103, 104, 106 (see col. 7, lines 1-46).

Tsujimoto does not expressly disclose that the error signal is generated using a maximum likelihood sequence estimation process.

Liang et al. disclose that the optimal solution to the problems of inter-symbol interference employs diversity combining and a maximum likelihood sequence estimator (col. 2, lines 50-56).

It would have been obvious to one of ordinary skill in the art to use a maximum likelihood sequence estimation process, as disclosed by Liang et al., in the diversity receiver of Tsujimoto for optimal correction of ISI.

Regarding claim 7, Tsujimoto discloses a receiver as disclosed above, and further teaches equalizing each of the replicas in feed forward equalizers 101, 102, combining the spatially equalized replicas to form a combined signal via combiner 158, generating a symbol error signal from the combined signal via circuit 109, temporally equalizing the combined signal via decision feedback equalizer 105, and adapting the spatial and temporal equalizing steps to the symbol error signal via tap control circuit 103, 104, 106 (see col. 7, lines 1-46).

Tsujimoto does not expressly disclose that the error signal is generated using a maximum likelihood sequence estimation process.

Liang et al. disclose that the optimal solution to the problems of inter-symbol interference employs diversity combining and a maximum likelihood sequence estimator (col. 2, lines 50-56).

It would have been obvious to one of ordinary skill in the art to use a maximum likelihood sequence estimation process, as disclosed by Liang et al., in the diversity receiver of Tsujimoto for optimal correction of ISI.

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18. Regarding claim 11, Tsujimoto discloses a receiver as disclosed above, and further teaches equalizing each of the diverse replicas in feed forward equalizers 101, 102, combining the spatially equalized replicas to form a combined signal via combiner 158, generating a symbol error signal from the combined signal via circuit 109, temporally equalizing the combined signal via decision feedback equalizer 105, and adapting the spatial and temporal equalizing steps to the symbol error signal via tap control circuit 103, 104, 106 (see col. 7, lines 1-46).

Tsujimoto does not expressly disclose that the error signal is generated using a maximum likelihood sequence estimation process.

Liang et al. disclose that the optimal solution to the problems of inter-symbol interference employs diversity combining and a maximum likelihood sequence estimator (col. 2, lines 50-56).

It would have been obvious to one of ordinary skill in the art to use a maximum likelihood sequence estimation process, as disclosed by Liang et al., in the diversity receiver of Tsujimoto for optimal correction of ISI.

### ***Conclusion***


Any inquiry concerning this communication or earlier communications from the examiner should be directed to David B. Lugo whose telephone number is 571-272-3043. The examiner can normally be reached on M-F; 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Lugo  
3/29/05

  
**KHAI TRAN**  
**PRIMARY EXAMINER**